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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,381	11/17/2003	Jochen Hoffmann	2003P54513US	4347

46798 7590 05/02/2005

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,381	HOFFMANN, JOCHEN	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,10,13-18 and 21-23* is/are rejected.

7)☒ Claim(s) *5,7-9,11,12,19,20 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, 10, 13-18 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lehmann (US 6,798,272).

3. With respect to claim 1, figures 1-7 of Lehmann teaches a shift register circuit, comprising:

a data input (215);

a plurality of stages (see figure 2), each comprising a data latch circuit (200) for storing a bit of data, a pointer latch circuit (214) for storing a bit of pointer information;

transfer circuitry (204) for serially transferring bits of data presented at the data input and to be stored in the data latch circuits through the plurality of stages during a first mode of operation; and

pointer advance circuitry for serially transferring one or more bits of pointer information forming a pointer through the plurality of stages during a second mode of operation without disturbing bits of data stored in the data latch circuits (203) (figure 2 of Lehmann shows the pointer circuitry directly connected to each other without having to go through the latch circuit).

4. With respect to claim 2, figure 3 of Lehmann discloses the pointer indicates, as selected, a stage having a pointer latch circuit storing a bit of a different logic level than a bit stored in a pointer latch circuit of a preceding stage.

5. With respect to claims 3 and 13, figure 6 of Lehmann discloses the pointer advance circuitry comprises, for each stage, a switched reset path (207) between a first node (205) of a pointer latch circuit and ground.

6. With respect to claim 4, figure 6 of Lehmann discloses the pointer advance circuitry is configured to advance a bit of pointer information from a first stage to a subsequent stage by closing the reset path (207).

7. With respect to claim 6, the apparatus of Lehmann teaches presetting the bit pointer (see column 2, lines 25-30).

8. With respect to claim 10, figures 1-7 of Lehmann disclose a fuse programming circuit for sequentially programming a plurality of fuses, comprising:

a shift register having a plurality of fuse latch circuits (200) for holding fuse programming data indicating which of the fuses are to be blown, a plurality of pointer latch circuits (214) for holding bits of a pointer for selecting one of the fuses, and pointer advance circuitry for serially advancing the pointer to select different fuses without disturbing bits of data stored in the data latch circuits; and

one or more blow circuits (719) configured to apply a blow voltage to a fuse (705) selected by the pointer if the fuse programming data stored in a corresponding fuse latch circuit indicates the selected fuse is to be blown.

9. With respect to claims 14 and 15, the prior art teach the pointer advance circuitry is configured to advance the pointer only when a bit in a fuse latch circuit corresponding to a currently selected fuse is at a predetermined logic level. (see column 2, lines 15-65).

10. With respect to claims 16-18 and 21-23, the methods therein are inherent given the apparatus of Lehmann as shown in the above rejections.

Allowable Subject Matter

11. Claims 5, 7-9, 11, 12, 14, 15, 19, 20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is an examiner's statement of reasons for allowance:

With respect to claims 5 and 24, the prior art does not teach the switched reset path comprises two serially connected transistors.

With respect to claim 6, the prior art does not teach circuitry for presetting the bit pointer.

With respect to claim 11, the prior art does not teach a blown clock signal.

With respect to claim 12, the prior art does not teach the pointer selects a fuse when a pointer latch circuit associated with fuse contains a bit of a first logic and fuse pointer latch associated with a previously selected fuse contains a bit of a second complementary logic level.

With respect to claims 7 and19, the prior art does not teach asynchronously advancing the pointer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

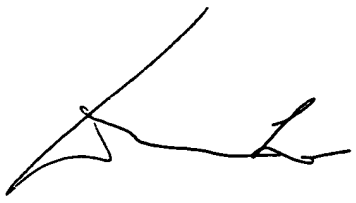
fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/28/2005



DON LE
PRIMARY EXAMINER